Session 20 Overview

WLAN/WPAN

Chair: Arya Behzad, Broadcom, San Diego, CA

Associate Chair: Jan Craninckx, IMEC, Leuven, Belgium

Mass consumer market wireless applications set strict requirements on cost, dynamic range, power consumption, and the number of external components used in the system. These constraints have already been applied to Bluetooth and 802.11b/g chips and the resultant chips have been reported at previous conferences. This year, we see these trends being applied to many other wireless standards such as multi-band WLAN ICs covering both the 2.4GHz band as well as the 4.9 to 5.8GHz band. At the same time authors present the first implementations of integrated multiple-antenna transceivers. Multiple-antenna techniques are used to increase the effective throughput of a wireless link as well as to increase the reliability and range of the connection. These issues are addressed in Papers 20.1 to 20.4.

On the other hand, Papers 20.5 to 20.8 address a variety of applications requiring very low power consumption for wireless connectivity. These applications include low-power home-control and industrial-automation systems utilizing the ZigBee standard as well as ultra-low-power autonomous sensor networks. In this session, several papers will present ICs addressing both of these markets.

In Paper 20.1, the authors present a 5GHz, 2×2 MIMO transceiver in 90nm CMOS supporting spatial multiplexing and diversity. Data rates of up to 108Mb/s can be achieved. Each RX consumes 120mA from a 1.4V supply. Each 3.3V 5GHz PA can deliver +13dBm average power with -27dB EVM in the 2×2 mode. The system-in-package includes microstrip front-end matching on a flip-chip package and incorporates a die with an area of 18mm^2.

An IEEE 802.11a/b/g wireless LAN SoC for low-power embedded applications is implemented in a 0.18µm CMOS technology and presented in Paper 20.2. The IC integrates the RF transceiver, digital PHY and MAC, CPU, and host interface. For 64QAM OFDM, the 5GHz/2.4GHz TX EVM is -27.4dB/-27.5dB at an output power of -5.2dBm/-3.5dBm. Overall 5GHz/2.4GHz RX sensitivity is -73dBm/-76dBm at 54Mb/s.

A transceiver for 802.11a/b/g access points which supports MRC diversity is presented in Paper 20.3. The diversity scheme results in a 3dB static sensitivity improvement over a single-receiver implementation. Receive ADCs and transmit DACs are included, allowing autonomous AGC and transmit power control loops and an all-digital modem/MAC IC. The 25mm^2 IC is fabricated in a 0.18µm CMOS process.

A highly linear up-conversion mixer with process insensitive gain control and gain insensitive output offset current is presented in Paper 20.4. A calibration scheme to remove the LO feed-through (LOFT) and I/Q imbalance is also introduced. The prototype achieves 3rd-order IMD suppression better than 52dBc, LOFT suppression better than 32dBc, and image-rejection better than 46dBc for all gain settings.

Paper 20.5 presents a 2.4GHz RF transceiver in 0.13µm CMOS for sensor networks. The transceiver operates from 400mV to accommodate a single-solar-cell power supply. The RX consumes 200 to 750µW and achieves a NF of 6.7dB and an IIP3 of -6.2dBm at 330µW. At 300µW output power, the PA is 44% efficient and the overall TX is 30% efficient.

A 0.18µm CMOS low-IF transceiver with integrated baseband processing that is compliant with the 802.15.4 ZigBee standard is described in Paper 20.6. The 5.77mm^2 die draws 14.7mA (RX) and 15.7mA (TX) while achieving -102dBm RX sensitivity and 3dBm TX power.

A low-power single-chip transceiver for the 430MHz ARIB STD-T67 narrowband systems is implemented in a 0.15µm CMOS technology and is presented in Paper 20.7. The chip integrates the entire radio including filters, a demodulator, and a microcontroller. The receive current of 10.8mA and the sensitivity of -120dBm at 1% BER is achieved in 2FSK operating at 2.4kb/s.

A fully integrated super-regenerative receiver in 0.13µm CMOS with on-chip quench generation is described in Paper 20.8. Auto-calibration improves the selectivity of a Q-enhanced filter and the sensitivity of super-regeneration. The prototype consumes 2.8mW, or 5.6nJ per received bit, at 500kb/s, and has a turn-on time of 83.6µs, a channel spacing of 10MHz, and a sensitivity of –90dBm.

 1-4244-0079-1/06/$20.00

20.1 A 5GHz 108Mb/s 2×2 MIMO Transceiver with Fully Integrated 16dBm PAs in 90nm CMOS **1:30 PM**
Y. Palaskas, Intel, Hillsboro, OR

A 5GHz 2×2 MIMO transceiver in 90nm CMOS supports spatial multiplexing and diversity, achieving 54/108Mb/s with -75/-63dBm sensitivity for an AWGN/25ns-Rayleigh channel, respectively. Each RX draws 120mA from a 1.4V supply. Each 3.3V 5GHz PA delivers +16/+13dBm average power with -25/-27dB EVM in 1×1/2×2 modes, respectively. The system-in-package including microstrip front-end matching on a flip-chip package occupies a die area of 18mm^2.

20.2 An 802.11a/b/g SoC for Embedded WLAN Applications **2:00 PM**
L. Nathawad, Atheros Communications, Irvine, CA

An 802.11a/b/g wireless LAN SoC for low-power embedded applications is implemented in a 0.18µm CMOS technology. The IC integrates the RF transceiver, digital PHY and MAC, CPU and host interface. For 64QAM OFDM, the 5GHz/2.4GHz TX EVM is -27.4dB/-27.5dB at an output power of -5.2dBm/-3.5dBm. Overall 5GHz/2.4GHz RX sensitivity is -73dBm/-76dBm at 54Mb/s.

20.3 A Wireless Transceiver with Integrated Data Converters for 802.11a/b/g Access Points **2:30 PM**
T. Montalvo, Analog Devices, Raleigh, NC

A transceiver for 802.11a/b/g access points supports MRC diversity resulting in a 3dB static sensitivity improvement over a single-receiver implementation. A closed-loop transmit power control scheme achieves 0.5dB accuracy. Receive ADCs and transmit DACs are included, allowing autonomous AGC and transmit power control loops and an all-digital modem/MAC IC. The 25mm^2 IC is fabricated in a 0.18µm CMOS process and achieves 3.9dB/4.5dB (low-band/high-band) receive NF and less than -35dB transmit EVM.

20.4 A Highly Linear Direct-Conversion Transmit Mixer Transconductance Stage with Local Oscillation Feedthrough and I/Q Imbalance Cancellation Scheme **3:15 PM**
C. Lee, Broadcom, San Diego, CA

A linear transconductance stage with process insensitive gain control and gain insensitive output offset current is proposed. A calibration scheme to remove the LO feedthrough (LOFT) and I/Q imbalance is also introduced. The prototype achieves 3rd-order IMD suppression better than 52dBc, LOFT suppression better than 32dBc, and image rejection better than 46dBc for all gain settings. The transmit chain achieves an 802.11a EVM of < -40dB.

20.5 An Ultra-Low-Power 2.4GHz RF Transceiver for Wireless Sensor Networks in 130nm CMOS with 400mV Supply and an Integrated Passive RX Front-end **3:30 PM**
B. Cook, University of California, Berkeley, CA

A 2.4GHz RF transceiver in 130nm CMOS for sensor networks is presented. The transceiver operates from 400mV to accommodate a single solar cell power supply. The RX dissipates 200 to 750µW and achieves a 6.7dB NF and a -6.2dBm IIP3 at 330µW. At 300µW output power, the PA is 44% efficient and the overall TX is 30% efficient.

20.6 A Fully Integrated 2.4GHz IEEE 802.15.4 compliant Transceiver for ZigBee Applications **3:45 PM**
W. Kluge, Atmel Germany, Dresden, Germany

A 0.18µm CMOS low-IF transceiver with integrated baseband processing according to IEEE 802.15.4 is described. The 5.77mm^2 die draws 14.7mA (RX) and 15.7mA (TX) while achieving -102dBm RX sensitivity and 3dBm TX power. The differential input 2.4mA RX RF-frontend provides 5.7dB system noise figure.

20.7 A 10.8mA Single-Chip Transceiver for 430MHz Narrowband Systems in 0.15µm CMOS **4:15 PM**
G. Hayashi, Matsushita, Osaka, Japan,

A low-power single-chip transceiver for 430MHz narrowband systems is implemented in a 0.15µm CMOS process. The chip integrates all the radio blocks including filters, a demodulator, and a microcontroller. The receive current of 10.8mA and the sensitivity of -120dBm at 1% BER are achieved in 2FSK operating at 2.4kb/s. The transceiver complies with the ARIB STD-T67.

20.8 A Fully Integrated Auto-Calibrated Super-Regenerative Receiver **4:45 PM**
J-Y. Chen, University of Michigan, Ann Arbor, MI

A fully integrated super-regenerative receiver in 0.13µm CMOS with on-chip quench generation is described. Auto-calibration improves the selectivity of a Q-enhanced filter and the sensitivity of super-regeneration. The prototype consumes 2.8mW, or 5.6nJ per received bit, at 500kb/s, and has a turn-on time of 83.6µs, a channel spacing of 10MHz, and a sensitivity of –90dBm.